FIG. 1 (PRIOR ART)

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FIG. 2
(PRIOR ART)

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FIG. 3 (PRIOR ART)

FIG. 4 (PRIOR ART)

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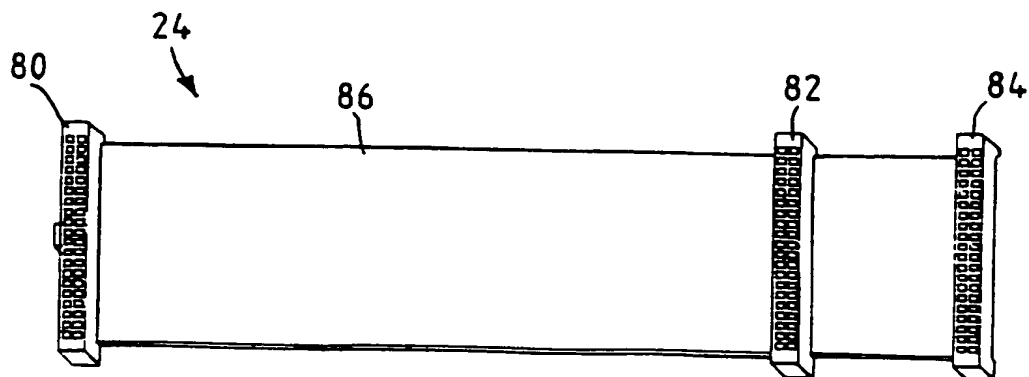MARSHALL, GERSTEIN & BORUN LLP 312/ 474-6300
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NAME	SOURCE	SIGNAL	PIN	PIN	SIGNAL	SOURCE	NAME
RESET	—	$\overline{\text{RESET}}$	1	2	GROUND		GROUND
DATA BUS BIT 7	I/O	DD7	3	4	DD8	I/O	DATA BUS BIT 8
DATA BUS BIT 6	I/O	DD6	5	6	DD9	I/O	DATA BUS BIT 9
DATA BUS BIT 5	I/O	DD5	7	8	DD10	I/O	DATA BUS BIT 10
DATA BUS BIT 4	I/O	DD4	9	10	DD11	I/O	DATA BUS BIT 11
DATA BUS BIT 3	I/O	DD3	11	12	DD12	I/O	DATA BUS BIT 12
DATA BUS BIT 2	I/O	DD2	13	14	DD13	I/O	DATA BUS BIT 13
DATA BUS BIT 1	I/O	DD1	15	16	DD14	I/O	DATA BUS BIT 14
DATA BUS BIT 0	I/O	DD0	17	18	DD15	I/O	DATA BUS BIT 15
GROUND	—	GROUND	19	20	N.C.		NO CONNECTION
DMA REQUEST	O	DMARQ	21	22	GROUND		GROUND
I/O WRITE	—	$\overline{\text{DIOW}}$	23	24	GROUND		GROUND
I/O READ	—	$\overline{\text{DIOR}}$	25	26	GROUND		GROUND
I/O CHANNEL READY	O	IORDY	27	28	SPSYNC: CSEL		SPINDLE SYNC or CABLE SELECT
DMA ACKNOWLEDGE	—	DMACK	29	30	GROUND		GROUND
INTERRUPT REQUEST	O	INTRQ	31	32	$\overline{\text{IOCS16}}$	O	16 BIT I/O
ADDRESS BIT 1	—	DA1	33	34	$\overline{\text{PDIAG}}$	—	PASSED DIAGNOSTIC
ADDRESS BIT 0	—	DA0	35	36	DA2	—	ADDRESS BIT 2
CHIP SELECT 0	—	$\overline{\text{CS1FX}}$	37	38	$\overline{\text{CS3FX}}$		CHIP SELECT 1
DRIVE ACTIVE/ DRIVE 1 PRESENT	O	$\overline{\text{DASP}}$	39	40	GROUND		GROUND

FIG. 5 (PRIOR ART)

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FIG. 6 (PRIOR ART)

COMMAND NAME	COMMAND CODE
NOP	00h
CFA REQUEST EXTENDED ERROR CODE	03h
DEVICE RESET	08h
READ SECTOR(S)	20h
WRITE SECTOR(S)	30h
CFA WRITE SECTORS WITHOUT ERASE	38h
READ VERIFY SECTOR(S)	40h
SEEK	70h
CFA TRANSLATE SECTOR	87h
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
PACKET	A0h
IDENTIFY PACKET DEVICE	A1h
SERVICE	A2h
SMART	B0h
CFA ERASE SECTORS	C0h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
READ DMA QUEUED	C7h
READ DMA	C8h
WRITE DMA	CAh
WRITE DMA QUEUED	CCh
CFA WRITE MULTIPLE WITHOUT ERASE	CDh
GET MEDIA STATUS	DAh
MEDIA LOCK	DEh
MEDIA UNLOCK	DFh
STANDBY IMMEDIATE	E0h
IDLE IMMEDIATE	E1h
STANDBY	E2h
IDLE	E3h
READ BUFFER	E4h
CHECK POWER MODE	E5h
SLEEP	E6h
FLUSH CACHE	E7h
WRITE BUFFER	E8h
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
SET FEATURES	EFh
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE LOCK	F5h
SECURITY DISABLE PASSWORD	F6h
READ NATIVE MAX ADDRESS	F8h
SET MAX ADDRESS	F9h
VENDOR SPECIFIC	9Ah,C0h-C3h,8xh,F0h,F7h,FAh-FFh
RETIRED	11h-1Fh,71h-7Fh,94h-99h, DBh-DDh,E9h
OBSOLETE	10h,21h-23h,31h-33h,3C,41h, 50h,C9h,CBh,EEh

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FIG. 7 (PRIOR ART)

IDE command and control register

CS1FX	CS3FX	DA2	DA1	DA0	READ ACCSESS	WRITE ACCSESS
COMMAND REGISTER BLOCK						
1	0	0	0	0	DATA REGISTER	DATA REGISTER
1	0	0	0	1	ERROR REGISTER	FEATURE REGISTER
1	0	0	1	0	SECTOR COUNT REGISTER	SECTOR COUNT REGISTER
1	0	0	1	1	SECTOR NUMBER REGISTER SECTOR NUMBER OR BLOCK ADDRESS 0-7	SECTOR NUMBER REGISTER SECTOR NUMBER OR BLOCK ADDRESS 0-7
1	0	1	0	0	CYLINDER REGISTER 0 CYLINDER 0-7 OR BLOCK ADDRESS 8-15	CYLINDER REGISTER 0 CYLINDER 0-7 OR BLOCK ADDRESS 8-15
1	0	1	0	1	CYLINDER REGISTER 1 CYLINDER 8-15 OR BLOCK ADDRESS 16-23	CYLINDER REGISTER 1 CYLINDER 8-15 OR BLOCK ADDRESS 16-23
1	0	1	1	0	DRIVE/HEAD REGISTER DRIVE/HEAD NUMBER OR BLOCK ADDRESS 24-27	DRIVE/HEAD REGISTER DRIVE/HEAD NUMBER OR BLOCK ADDRESS 14-31
1	0	1	1	1	STATUS REGISTER	COMMAND REGISTER
CONTROL REGISTER BLOCK						
0	1	0	0	0	NOT USED	NOT USED
0	1	0	0	1	NOT USED	NOT USED
0	1	0	1	0	NOT USED	NOT USED
0	1	0	1	1	NOT USED	NOT USED
0	1	1	0	0	NOT USED	NOT USED
0	1	1	0	1	NOT USED	NOT USED
0	1	1	1	0	ALTERNATE STATUS REGISTER	CONTROL REGISTER
0	1	1	1	1	ADDRESS REGISTER	NOT USED

ADDRESS — NAME AND FUNCTION

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IDE status register

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

FIG. 8 (PRIOR ART)

IDE error register

7	6	5	4	3	2	1	0
BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF

FIG. 9 (PRIOR ART)

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FIG. 10A

FIG. 10B

FIG. 10C

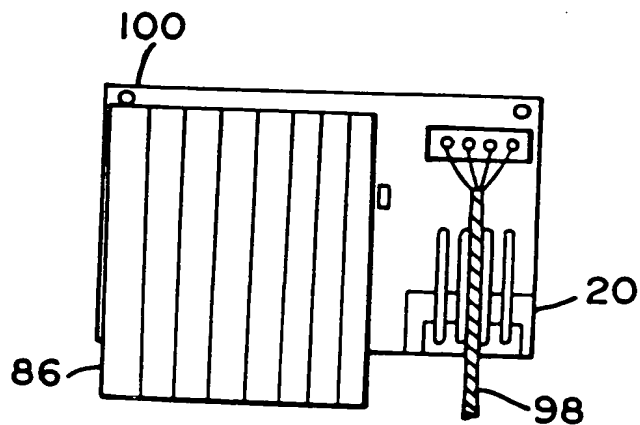**FIG. 10 D**

FIG. 10E

FIG. 11A

100

20

86

98

FIG. 11B

86

98

100

20

100

20

86

98

FIG. 11C

FIG. IID

FIG. IIE

FIG. 12

FIG. 13

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INVALID
COMMAND
GENERATOR — 136

D7   D5   D3   D1
   D6   D4   D2   D0

FIG. 14

132

BUS { DD0
156   ·
      ·
      DD7   184   ·   ·   ·

180   186
1OE

BUS   BUS { D0
154   160   ·   188
             ·
             D7

             190
2OE
182

DD0 } BUS
·   158
·
DD7

FIG. 15

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ADDRESS
VALID

192

$\overline{DIOR}$
$\overline{DIOW}$

193

194

DATA
VALID

196

198

199

FIG. 16

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CPU 10

200	202	204	208
SET UP REGISTER BLOCK	SEND COMMAND	WRITE SECTOR BUFFER	READ STATUS

HARD DISK DRIVE 20

206
WRITE SECTOR

DRDY

BSY

DRQ

ERR

ABRT

INTRQ

FIG. 17

CPU 10

SET UP REGISTER BLOCK	ATTEMPT TO SEND COMMAND	READ STATUS

210   212   214

HARD DISK
DRIVE 20

DRDY

BSY

DRQ

ERR

ABRT

INTRQ

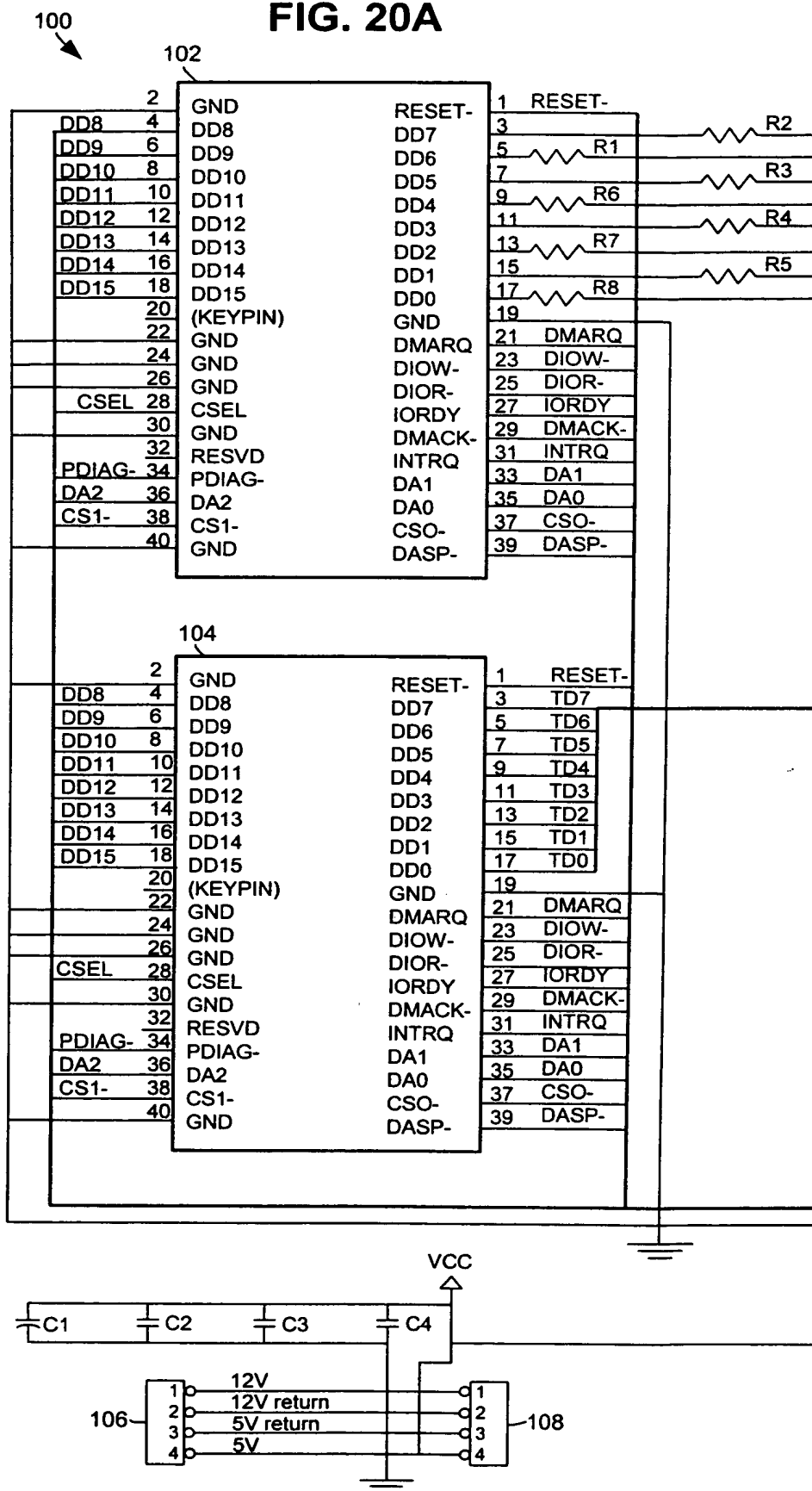FIG. 18

FIG. 19

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FIG. 20A

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FIG. 20B

FIG. 21